IN THE CLAIMS

Claim 1 (currently amended): A DC/DC converter comprising:

an input to which an input voltage (Vin) is applied,

an inductance (L) whose one terminal is connected to said input,

a first controllable switch (N1) via which the other terminal of said inductance (L) is connectable to a reference potential (Vss),

a second controllable switch (P1) via which the other terminal of said inductance (L) is connectable to the output of said converter, and

a regulator circuit (1) configured so that it is able to control said two switches (N1, P1) in regulating the output voltage (Vout) of said DC/DC converter to a predetermined wanted value, said second controllable switch being a PMOS-FET and said regulator circuit (1) being configured so that when said input voltage (Vin) is higher than said wanted value of said output voltage, ~~the~~ a gate of said PMOS-FET (P1) is permanently connected to a voltage which is larger than the difference between said input voltage and the threshold voltage of said PMOS-FET, connecting said back gate of said PMOS-FET permanently to a voltage which is larger than the expression input voltage plus threshold voltage of said PMOS-FET minus diode voltage of a pn junction of said PMOS-FET and timing said first controllable switch (N1) with a specific duty cycle so that said output voltage attains said wanted value.

Claim 2 (original): The DC/DC converter as set forth in Claim 1, wherein said first controllable switch is a NMOS-FET.

Claim 3 (original): The DC/DC converter as set forth in Claim 2, wherein both MOS-FETs are AUTO OFF.

Claim 4 (original): The DC/DC converter as set forth in Claim 1, wherein said regulator circuit is configured so that when said input voltage is higher than said wanted value of said output voltage, the gate of said PMOS-FET is permanently connected to said input voltage.

Claim 5 (original): The DC/DC converter as set forth in Claim 2, wherein said regulator circuit is additionally configured so that when said input voltage is lower than the wanted value of said output voltage, the gates of said NMOS-FET and PMOS-FET can be alternatingly timed to connect the output voltage of said DC/DC converter and said reference potential with a specific duty cycle so that the output voltage of said DC/DC converter attains said wanted value.

Claim 6 (original): The DC/DC converter as set forth in Claim 1, wherein the back gate of said PMOS-FET is connected to the drain of a further PMOSFET, the source of said further PMOS-FET being connected to the output of said DC/DC converter and the back gate of said further PMOS-FET to its drain and said regulator circuit being configured so that when said input voltage is higher than the wanted value of said output voltage, the gate of said further PMOS-FET is permanently connected to said input voltage.

Claim 7 (original): The DC/DC converter as set forth in Claim 1, wherein in addition a storage capacitor is provided between the output of said DC/DC converter and reference potential.

Claim 8 (original): The DC/DC converter as set forth in Claim 1, wherein said reference potential is ground.

Claim 9 (original): A method for DC voltage conversion by a DC/DC converter comprising:

an input to which an input voltage is applied,

a inductance whose one terminal is connected to said input,

a first controllable switch via which the other terminal of said inductance is connectable to a reference potential, and

a second controllable switch in the form of a PMOS-FET via the source-drain circuit of which the other terminal of said inductance is connectable to the output of said converter,

wherein when said input voltage of said DC/DC converter exceeds the wanted value of said output voltage, the gate of said PMOS-FET is permanently connected to a voltage which is larger than the difference between said input voltage and said threshold voltage of said PMOS-FET, the back gate of said PMOS-FET is permanently connected to a voltage which is larger than the expression input voltage plus threshold voltage of said PMOS-FET minus diode voltage of a pn junction of said PMOS-FET and said first controllable switch is timed with a specific duty cycle so that said output voltage attains said wanted value.

Claim 10 (original): The method as set forth in Claim 9 wherein said first controllable switch is a NMOS-FET.

Claim 11 (original): The method as set forth in Claim 10 wherein when said input voltage is lower than a predetermined wanted value for said output voltage of said DC/DC converter, said two controllable switches are timed with a specific duty cycle opposingly so that said output voltage attains said wanted value, said output voltage of said DC/DC converter and said reference potential being applied alternatingly to the gates of said PMOS-FET and of said NMOS-FET.